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PATENT 01AB067

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Date: 8-25-04 Himanshu S. Amin

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:			
Applicant(s):	Raymond R. Husted, *et al.*	Examiner:	Jasmine Song
Serial No:	09/915,024	Art Unit:	2188
Filing Date:	July 25, 2001		

Title: SYSTEM AND METHOD FOR INDUSTRIAL CONTROLLER WITH AN I/O PROCESSOR USING CACHE MEMORY TO OPTIMIZE EXCHANGE OF SHARED DATA

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

Dear Sir:

Applicants submit this brief in triplicate in connection with an appeal of the above-identified patent application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [ALBRP226US].

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I. Real Party in Interest (37 C.F.R. §1.192(c)(1))

The real party in interest in the present appeal is Rockwell Automation Technologies, Inc., the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §1.192(c)(2))

Appellants, appellants' legal representative, and/or the assignee of the present application are not aware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §1.192(c)(3))

Claims 1-19 are pending in the application. The rejection of claims 1-19 is being appealed.

IV. Status of Amendments (37 C.F.R. §1.192(c)(4))

No claim amendments have been entered after the Final Office Action.

V. Summary of Invention (37 C.F.R. §1.192(c)(5))

The present invention relates to methods and systems for I/O forcing using an I/O processor having cache memory, wherein a processor and an I/O processor are operatively coupled to a shared memory that stores, for example, configuration data, I/O force data, output data effecting control of the process and/or input data representative of the status of the controlled process. *See* page 3, lines 12-18. Further, the invention as claimed provides that the I/O processor is operatively coupled to a cache memory, and that the operatively coupled cache memory can be selectively loaded with at least a portion of the I/O force data stored in the shared memory. In addition, the I/O processor not only stores information associated with inputs in the shared memory based in part upon the inputs received from sensing devices and I/O force data stored in the cache memory, but also affects control of the process based at least in part upon output information retrieved from the shared memory and I/O force data stored in the cache memory. *See* page 3, lines 19-26. Moreover, the claimed invention provides for the associated processor to notify the I/O processor whenever I/O force data is altered during

control program execution, thus allowing the I/O/ processor to refresh the cache memory after receipt of the notification. *See* page 3, lines 28-31.

VI. Statement of the Issues (37 C.F.R. §1.192(c)(6))

A. Whether claims 1-19 are unpatentable under 35 U.S.C. §103(a) over Schmidt *et al.* (US 5,212,631) in view of Sharma *et al.* (US 6,085,263).

VII. Grouping of Claims (37 C.F.R. §1.192(c)(7))

For purposes of this appeal only, the claims are grouped as follows:

Claims 1-19 stand or fall together.

VIII. Argument (37 C.F.R. §1.192(c)(8))

A. Rejection of Claims 1-19 Under 35 U.S.C. §103(a)

Claims 1-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Schmidt *et al.* (US 5,212,631) in view of Sharma *et al.* (US 6,085,263). Reversal of this rejection is respectfully requested for at least the following reasons.

i. Schmidt et al. and Sharma et al., alone or in combination, fail to teach or suggest all the limitations set forth in the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***. *See* MPEP §706.02(j). The ***teaching or suggestion to make the claimed combination*** and the reasonable expectation of success ***must be found in the prior art and not based on the Applicant's disclosure***. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

Independent claim 1 recites *an I/O processor for performing at least one of input and output functions, the I/O processor and the processor operatively coupled to the shared memory, the* ***I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values stored in the shared memory, the I/O processor storing input values in the shared memory based at least in part upon forced I/O values stored in the cache memory****, the I/O processor determining output values based at least in part upon forced I/O values stored in the cache memory.* Independent claims 6 and 9 recite similar limitations. It is apparent therefore that the invention as claimed in independent claims 1, 6 and 9 sets forth an I/O processor operatively coupled to a shared memory and a cache memory, wherein at least a portion of the forced I/O values in the shared memory are also stored in the cache memory. The I/O processor, in addition, stores input values in shared memory based at least in part on the forced I/O values that are stored in the cache memory, as well as, determining output values based at least in part upon the forced I/O values that are stored in the cache memory. Both Schmidt *et al.* and Sharma *et al.*, either alone or in combination, are silent regarding these novel features of the invention as claimed.

In the Final Office Action dated February 24, 2004, it was conceded by the Examiner that Schmidt *et al.* failed to teach or suggest an: "I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values stored in shared memory ... storing input values in the shared memory and determining output values based at least in part upon forced I/O values stored in the cache memory." *Id.* at page 3. Applicants' representative further noted, in both the Reply to the Final Office Action dated February 24, 2004, as well as the Reply to Advisory Action dated May 11, 2004, that in addition to the deficiency identified by the Examiner, that both Schmidt *et al.* and Sharma *et al.* failed to teach or suggest the novel limitation of the I/O processor determining whether or not to store input values in the shared memory ***based at least in part upon forced I/O values stored in the cache memory***. Thus, the fact that both Schmidt *et al.* and Sharma *et al.* fail to teach or suggest the deficiency identified by applicants' representative alone is grounds for allowance of the subject claims.

Nevertheless, in order to fully address the issues raised in the Final Office Action dated February 24, 2004, regarding the assertion that Sharma *et al.* rectified the

deficiency identified by the Examiner with respect to independent claims 1, 6 and 9, *viz.* Schmidt *et al.* does not teach or suggest ***the I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values stored in the shared memory***. Applicants' representative had argued in the Reply to Advisory Action dated May 11, 2004, an reiterates herein, that the passage to which the Examiner cites, i.e. col. 14, lines 9-37, is silent regarding the subject limitation. Nowhere in the cited passage is mention made of an I/O processor coupled to a cache memory ***storing at least a portion of the forced I/O values stored in the shared memory***. Sharma *et al.* at best can be characterized as disclosing a *prefetch controller* coupled to a cache memory; the *prefetch controller* utilizing cache memory references to compare memory references at the head of an input queue with memory addresses stored in the cache memory. Sharma *et al.* does not teach or suggest using a shared memory to store ***forced I/O values***, let alone storing a ***at least a portion of the forced I/O values*** that are stored in the shared memory in the cache memory. Thus, it is submitted that Sharma *et al.* fails to make up for the deficiencies presented by Schmidt *et al.*, as neither teach nor suggest, either alone or in combination, all the limitations set forth in the subject claims. Accordingly, withdrawal of the rejection of independent claims 1, 6 and 9, and associated dependent claims, is respectfully requested.

With respect to independent claims 10 and 17. Independent claims 10 and 17 recite similar claim limitations: ***forcing the input or output based at least in part upon the forcing information loaded in the cache***. As the Examiner conceded in the Final Office Action dated February 24, 2004, Schmidt *et al.* fails to teach or suggest this novel limitation of the claimed invention. *See* page 4. In order to make up for this deficiency, the Examiner directed applicants' representative to Sharma *et al.*, col. 14, lines 9-37.

As was stated by applicants' representative in the Reply to Advisory Action dated May 11, 2004, and is restated herein, Sharma *et al.* at the passage indicated by the Examiner, fails to teach or suggest utilizing at least part of the information contained within a cache memory to force input or output. Nowhere in Sharma *et al.* is this exemplary facility intimated. It is submitted that Sharma *et al.* at best discloses the utilization of cache memory to compare whether or not memory references at the head of an input queue are stored within the cache memory. Sharma *et al.* does not disclose

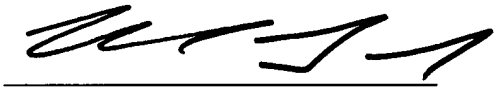
utilizing the cache in the exemplary manner as recited in the subject claims. Accordingly, in view of at least the foregoing, it is believed that the subject claims are in condition for allowance and thus it is respectfully requested that the rejection of independent claims 10 and 17, and claims that depend there from, should be withdrawn.

IX. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-19 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Respectfully submitted,
AMIN & TUROCY, LLP



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X. Appendix of Claims (37 C.F.R. §1.192(c)(9))

1. A programmable control system, comprising:

a processor for executing a control program;

a shared memory storing data associated with the control program, at least one of data associated with sensing and actuating devices, and forced I/O values; and,

an I/O processor for performing at least one of input and output functions, the I/O processor and the processor operatively coupled to the shared memory, the I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values stored in the shared memory, the I/O processor storing input values in the shared memory based at least in part upon forced I/O values stored in the cache memory, the I/O processor determining output values based at least in part upon forced I/O values stored in the cache memory.

2. The programmable control system of claim 1, the processor sending a message to the I/O processor in the event a forced I/O value has been altered during execution of the control program, the I/O processor causing the cache memory to be refreshed in response to receipt of the message.

3. The programmable control system of claim 1, the I/O processor performing a blocked write to refresh the cache memory in response to receipt of a message.

4. The programmable control system of claim 1, the forced I/O values comprising at least one of binary and analog values.

5. The programmable control system of claim 1, the processor and I/O processor being coupled by at least one of a serial communications backplane bus, a parallel communications backplane bus and a network.

6. A programmable control system, comprising:

a processor for executing a control program;

a shared memory storing data associated with the control program and infrequently changed data; and,

an I/O processor for performing at least one of input and output functions, the I/O processor and the processor operatively coupled to the shared memory, the I/O processor operatively coupled to a cache memory storing at least a portion of the infrequently changed data stored in the shared memory, the I/O processor utilizing the infrequently changed data stored in the cache memory.

7. The programmable control system of claim 6, the infrequently changed data being at least one of I/O force data, configuration data, I/O fail safe information, a connection table, an output keep alive table and information associated with an input time-out.

8. The programmable control system of claim 6, the processor sending a message to the I/O processor in the event the infrequently changed data has been altered during execution of the control program, the I/O processor causing the cache memory to be refreshed in response to receipt of the message.

9. A programmable control system, comprising:

means for executing a control program;

means for storing data representing status of at least one of sensing and actuating devices, the means for storing further storing data associated with forced values for the at least one of sensing and actuating devices;

means for performing at least one of input and output functions, the means for performing at least one of input and output functions and the means for executing a control program operatively coupled to the means for storing data, the means for performing at least one of input and output functions operatively coupled to a cache memory means storing at least a portion of the data associated with forced values for the at least one of sensing and actuating devices, the means for performing at least one of input and output functions storing input values in the memory means based at least in part

upon forced I/O values stored in the cache memory means, the means for performing at least one of input and output functions determining output values based at least in part upon forced I/O values stored in the cache memory.

10. A method for forcing an I/O values in an industrial control environment, comprising:

loading a cache with forcing information associated with a forced input or output;

receiving information associated with an input from a sensing device;

retrieving information associated with an output to an actuating device; and,

forcing the input or output based at least in part upon the forcing information loaded in the cache.

11. The method of claim 10, further comprising:

refreshing the cache if the forcing information is altered during control program execution.

12. The method of claim 10, loading the cache with forcing information comprising retrieving forcing information from a shared memory and loading the forcing information into the cache using an I/O processor.

13. The method of claim 12, retrieving forcing information from the shared memory comprising receiving a message in the I/O processor indicating that the forcing information in the shared memory has been altered, and refreshing at least a portion of the cache with the altered forcing information.

14. The method of claim 13, refreshing at least a portion of the cache comprising reading the altered forcing information from the shared memory and performing a blocked write to refresh the cache memory with the altered forcing information.

15. The method of claim 12, forcing the input comprising providing a forced input to the shared memory based on the forcing information using the I/O processor.

16. The method of claim 12, forcing the output comprising providing a forced output to the actuating device based on the forcing information using the I/O processor.

17. A method of selectively forcing I/O in a control system having an I/O processor and a control processor associated with a shared memory, the method comprising:

selectively storing a forced input value to the shared memory according to forcing information in a cache associated with the I/O processor;

selectively providing a forced output value to an actuating device according to the forcing information in the cache using the I/O processor; and

obtaining altered forcing information from the shared memory using the I/O processor and storing the altered forcing information in the cache according to a message from the control processor.

18. The method of claim 17, storing the altered forcing information in the cache comprising refreshing the cache by writing the altered forcing information to a virtual memory location.

19. The method of claim 17, comprising writing the altered forcing information to the shared memory and sending the message to the I/O processor using the control processor, the message indicating alteration of the forcing information in the shared memory.